UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,594	08/19/2003	Nobuyasu Kanekawa	056207.50307C1	2784

23911 7590 05/04/2005

CROWELL & MORING LLP
INTELLECTUAL PROPERTY GROUP
P.O. BOX 14300
WASHINGTON, DC 20044-4300

EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/642,594	KANEKAWA ET AL.
	Examiner	Art Unit
	Thomas L. Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,17 and 18* is/are rejected.

7)☐ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/943,384.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/17/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/17/05 has been entered.

Information Disclosure Statement

2. The Information Disclosure Statement filed on 03/17/2005 has been considered.

Claim Objections

3. Claims 15-19 are objected to because of the following informalities: In claim 15, lines 11-12, there is no apparent antecedent basis for "said power semiconductor elements." Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by TAKAGI ET AL. (6,130,458).

Takagi et al. discloses a semiconductor device with an embedded insulation layer 10 formed in a semiconductor substrate14; a plurality of power semiconductor transistors 2-4 formed on said semiconductor substrate14; a trench 12 isolating between said plurality of power semiconductor transistors 2-4 formed on said semiconductor substrate14 on said embedded insulation layer 10, whereby said plurality of semiconductor transistors 2-4 are individually isolated (2 is isolated from 1 by trench 12 and vice-versa) from each other and isolated from any other (the "any other," in this case, being transistors 5L,6L,7L,5H,6H, and 7H. Note that, by the terms of claim 15, the trench 12 is only required to isolate the

"any other," from the plurality of power semiconductor transistors. The trench need not isolate the "any other," amongst themselves) semiconductor transistors; an isolator 47-48 (note figure 10A) insulating and driving control electrodes (not marked, seen just above bases 22 in transistors 2 and 4) of a pair of power semiconductor elements (the transistors 2 and 4); and wherein at least two (the at least two being transistors 2 and 4) of said plurality of power semiconductor transistors 2-4 are each connected (see figure 10A) to each other in series. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claim 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over TAKAGI ET AL. (6,130,458) in view of MIURA (4,993,396).

Takagi et al. discloses a semiconductor device with all the limitations of claim 16 except an ignition coil driven by the power semiconductor transistors. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

However, Miura discloses a semiconductor device with an ignition coil 2 driven by power semiconductor transistor 1. Note figure 1 and column 4 lines 27-

46 of Miura. Therefore, it would have been obvious to a person having skill in the art to use the power semiconductor transistors of Takagi et al.'s semiconductor device to drive an ignition coil such as taught by Miura because power semiconductor transistors have a faster rise time and generate higher voltages into inductive loads such as ignition coils.

B. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over TAKAGI et al. (6,130,458) in view of FOERSTER (5,828,141).

Takagi et al. discloses a semiconductor device with all the limitations of claim 16 except a fuel injector driven by the power semiconductor transistors. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

However, Foerster discloses a semiconductor device with a fuel injector driven by power semiconductor transistors. Note figure 1 and column 1 lines 32-35 of Foerster. Therefore, it would have been obvious to a person having skill in the art to having skill in the art to use the power semiconductor transistors of Takagi et al.'s semiconductor device with the fuel injector driven by power semiconductor transistors such as taught by Foerster in order to demagnetize the inductive load presented by the fuel injector as rapidly as possible, in a repeatable fashion.

C. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over TAKAGI ET AL. (6,130,458) in view of ENDO ET AL. (6,225,664) (cited by the applicant).

Takagi et al. discloses a semiconductor device with all the limitations of claim 16 except an input control circuit supplying a control signal of a specific control pattern to control electrodes of a plurality of power semiconductor transistors on the base of input signals. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

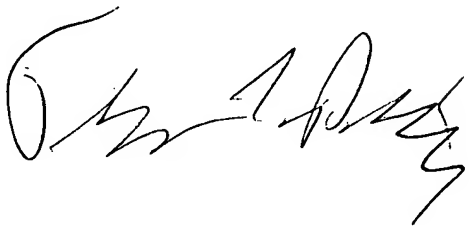
However, Endo et al. discloses a semiconductor device with an input control circuit 131-132 supplying a control signal (via buffers 121-122) of a specific control pattern to control electrodes N_{u1} and N_{d1} of a plurality of power semiconductor transistors Q_{u1} and Qd_1 on the base of input signals. Note figure 6 of and column 13 lines 28-32 of Endo et al. Therefore, it would have been obvious to a person having skill in the art to augment Takagi et al.'s semiconductor device with the input control circuit supplying a control signal of a specific control pattern to control electrodes of a plurality of power semiconductor transistors on the base of input signals such as taught by Endo et al. in order to supply a control signal to the power semiconductor transistors to thus provide a controlled output from the power semiconductor transistors.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
05/05